WHAT IS CLAIMED IS:

1. A power semiconductor device comprising:

a first semiconductor layer of non-doped $Al_XGa_{1-X}N$ ($0 = X = 1$);

a second semiconductor layer of non-doped or n-type $Al_YGa_{1-Y}N$ ($0 = Y = 1$, $X < Y$) disposed on the first semiconductor layer;

source and drain electrodes disposed separately from each other, and electrically connected to the second semiconductor layer;

a gate electrode disposed on the second semiconductor layer between the source and drain electrodes;

an insulating film covering the second semiconductor layer between the gate and drain electrodes;

a first field plate electrode disposed on the insulating film and electrically connected to the gate electrode; and

a second field plate electrode disposed on the insulating film and electrically connected to the source electrode.

2. The device according to claim 1, wherein the second field plate electrode comprises an intermediate electrode portion interposed between the first field plate electrode and the drain electrode.

3. The device according to claim 2, wherein the insulating film comprises a first insulating film disposed on the second semiconductor layer, and

the first field plate electrode and the intermediate electrode portion are disposed on the first insulating film.

4. The device according to claim 3, wherein the second field plate electrode comprises a covering electrode portion that connects the source electrode to the intermediate electrode portion and covers the first field plate electrode through an inter-level insulating film.

5. The device according to claim 1, wherein the second field plate electrode comprises a covering electrode portion that covers the first field plate electrode through an inter-level insulating film and has a distal end extending beyond the first field plate electrode toward the drain electrode.

6. The device according to claim 1, wherein the insulating film has first and second thicknesses below the first and second field plate electrodes, respectively, and the second thickness is larger than the first thickness.

7. The device according to claim 6, wherein the insulating film comprises a first insulating film disposed on the second semiconductor layer and a second insulating film disposed on the first insulating film, the first field plate electrode is disposed on the first insulating film, and the second field plate electrode is disposed on the second insulating film.

8. The device according to claim 1, further comprising a third field plate electrode disposed on the insulating film and electrically connected to the drain electrode.

9. The device according to claim 8, wherein the insulating film comprises a first insulating film disposed on the second semiconductor layer, and the first and third field plate electrodes are disposed on the first insulating film.

10. The device according to claim 8, wherein the insulating film comprises a first insulating film disposed on the second semiconductor layer and a second insulating film disposed on the first insulating film, the first field plate electrode is disposed on the first insulating film, and the third field plate electrode includes a portion disposed on the second insulating film.

11. A power semiconductor device comprising:

a first semiconductor layer of non-doped $Al_XGa_{1-X}N$ ($0 = X = 1$);

a second semiconductor layer of non-doped or n-type $Al_YGa_{1-Y}N$ ($0 = Y = 1$, $X < Y$) disposed on the first semiconductor layer;

first and second contact layers of n-type $Al_ZGa_{1-Z}N$ ($0 = Z = 1$) disposed separately from each other on or in a surface of the second semiconductor layer, and having a resistivity lower than that of

the second semiconductor layer;

source and drain electrodes disposed on the first and second contact layers, respectively;

a gate electrode disposed on the second semiconductor layer between the source and drain electrodes;

an insulating film covering the second semiconductor layer between the source and drain electrodes;

a first field plate electrode disposed on the insulating film and electrically connected to the source electrode; and

a second field plate electrode disposed on the insulating film and electrically connected to the drain electrode.

12. The device according to claim 11, wherein the first and second contact layers are formed in the surface of the second semiconductor layer, and extend beyond an interface between the first and second semiconductor layers into the first semiconductor layer.

13. The device according to claim 11, wherein the first and second contact layers protrude on the surface of the second semiconductor layer on a side opposite to the first semiconductor layer.

14. The device according to claim 11, further comprising a third semiconductor layer of p-type $Al_XGa_{1-X}N$ ($0 = X = 1$) disposed on the first semiconductor layer on a side opposite to the second

semiconductor layer.

15. The device according to claim 14, wherein the third semiconductor layer is electrically connected to the source electrode.

16. The device according to claim 11, wherein a ratio between first and second projected lengths in a direction connecting the source and drain electrodes is set to be 0.9 to 1.1, where the first projected length denotes a portion of the first field plate electrode that extends beyond an end of the gate electrode toward the drain electrode, and the second projected length denotes a portion of the second field plate electrode on the insulating film.

17. The device according to claim 16, wherein the second projected length is set larger than a thickness of the first semiconductor layer.

18. A power semiconductor device comprising:

a first semiconductor layer of non-doped $Al_XGa_{1-X}N$ ($0 = X = 1$);

a second semiconductor layer of non-doped or n-type $Al_YGa_{1-Y}N$ ($0 = Y = 1$, $X < Y$) disposed on the first semiconductor layer;

source and drain electrodes disposed separately from each other, and electrically connected to the second semiconductor layer;

a gate electrode disposed on the second semiconductor layer between the source and drain electrodes;

an insulating film disposed on the second semiconductor layer between the source and drain electrodes, and covering the gate electrode;

a first field plate electrode disposed on the insulating film and electrically connected to the source electrode;

a second field plate electrode disposed on the insulating film and electrically connected to the drain electrode; and

a drain contact electrode disposed in contact with the first and second semiconductor layers at a position adjacent to the drain electrode, and electrically connected to the drain electrode.

19. The device according to claim 18, wherein the drain contact electrode is disposed in a trench that extends from a surface of the second semiconductor layer through an interface between the first and second semiconductor layers into the first semiconductor layer.

20. The device according to claim 18, further comprising a source contact electrode disposed in contact with the first and second semiconductor layers at a position adjacent to the source electrode, and electrically connected to the source electrode.

21. The device according to claim 20, wherein the source contact electrode is disposed in a trench that extends from a surface of the second semiconductor

layer through an interface between the first and second semiconductor layers into the first semiconductor layer.

22. The device according to claim 18, further comprising first and second contact layers of n-type $Al_ZGa_{1-Z}N$ (0 = Z = 1) disposed separately from each other on the second semiconductor layer, and having a resistivity lower than that of the second semiconductor layer, wherein the source and drain electrodes are disposed on the first and second contact layers, respectively.